AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. (currently amended) The apparatus of claim ~~1~~ 38 further comprising a control circuit coupled to the ~~plurality of~~ transmission ~~circuits~~ circuit, to the ~~plurality of~~ receiving ~~circuits~~ circuit and to the ~~plurality of~~ parallel-serial conversion ~~circuits~~ circuit, the control circuit to control conversion of signals between parallel and serial formats and to control transmission and receiving of data.

3. (currently amended) The apparatus of claim ~~1~~ 38, wherein ~~at least one of~~ the ~~plurality of~~ parallel-serial conversion circuits ~~receives~~ is further operable to convert SONET/SDH framed data, whose bits are received from the parallel input/output line at a first bit rate, from ~~as~~ a parallel signal ~~and converts the parallel signal~~ to a corresponding serial signal at the first bit rate.

4. (currently amended) The apparatus of claim 3, wherein ~~one of~~ the ~~plurality of~~ transmission ~~circuits~~ circuit transmits the converted serial signal at the first bit rate.

Claims 5-6 (canceled)

7. (currently amended) The apparatus of claim ~~1~~ 38, wherein ~~at least one of~~ the ~~plurality of~~ parallel-serial conversion ~~circuits~~ circuit receives a serial signal at a ~~first~~ received bit rate and converts the serial signal to a parallel SONET/SDH framed data at the ~~first~~ received bit rate.

8. (currently amended) The apparatus of claim 7, wherein ~~one of~~ the ~~plurality of~~ receiving ~~circuits~~ circuit receives the serial signal at the ~~first~~ received bit rate and sends the serial signal to the parallel-serial conversion circuit.

9. (currently amended) The apparatus of claim ~~1~~ 38, wherein ~~one of~~ the ~~plurality of~~ parallel-serial conversion ~~circuits~~ circuit receives multiple serial signals at a ~~first~~ received bit rate and converts the serial signals to parallel SONET/SDH framed data at a ~~second~~ bit rate, ~~where the second bit rate~~ which is greater than the ~~first~~ received bit rate.

10. (previously presented) The apparatus of claim 9, wherein one of the receive circuits receives the multiple serial signals at the first bit rate.

11. (currently amended) A method comprising:

configuring a backplane to communicatively connect a cross-connect card to a device interface card;

receiving bits in a parallel signal at a first bit rate;

converting the parallel signal into multiple serial signals; and

transmitting the multiple serial signals including the received bits over a the backplane at a second bit rate, thereby communicating data between the cross-connect card and the device interface card, wherein the second bit rate being is different than the first bit rate,

wherein stuffing data is added to the received bits in the multiple serial signals such that the number of the multiple serial signals multiplied by the first bit rate is equal to the second bit rate,

wherein the bits are received as SONET/SDH framed data in the parallel signal, and

wherein the converting of the parallel signal into the multiple serial signals allows the backplane to be less complex.

Claims 12-13 (canceled)

14. (previously presented) The method of claim 11 further comprising transmitting the multiple serial signals at the second bit rate using both a first transmitting circuit and a second transmitting circuit.

15. (currently amended) A method comprising:

configuring a backplane to communicatively connect a cross-connect card and a device interface card;

receiving bits in multiple serial signals at a first bit rate from a—the backplane, the received bits representing data communicated between the cross-connect card and the device interface card;

converting the multiple serial signals to a parallel signal;

transmitting the parallel signal including the received bits at a second bit rate, wherein the first bit rate is greater than the second bit rate,

wherein stuffing data is removed from at least one of the multiple serial signals during conversion such that the number of the multiple serial signals multiplied by the second bit rate is equal to the first bit rate,

wherein the bits are SONET/SDH framed data in the parallel signal, and

wherein the receiving of bits in serial signals allows the backplane to be less complex.

Claims 16-17 (canceled)

18. (previously presented) The method of claim 15 further comprising receiving the multiple serial signals at the first bit rate using both a first receiving circuit and a second receiving circuit.

19. (currently amended) An apparatus comprising:

a backplane communicatively connecting a cross-connect card to a device interface card;

means for receiving bits of a parallel signal at a first bit rate;

means for converting the parallel signal into multiple serial signals; and

means for transmitting the multiple serial signals including the received bits at a second bit rate over ~~a~~ the backplane, thereby communicating data between the cross-connect card and the device interface card, wherein the second bit rate ~~being~~ is different than the first bit rate,

wherein stuffing data is added to the received bits in the multiple serial signals such that the number of the multiple serial signals multiplied by the first bit rate is equal to the second bit rate,

wherein the bits are received as SONET/SDH framed data in the parallel signal, and

wherein the converting of the parallel signal into the multiple serial signals allows the backplane to be less complex.

Claims 20-21 (canceled)

22. (previously presented) The method of claim 19 further comprising means for transmitting the serial signals at the second bit rate using both a first transmitting circuit and a second transmitting circuit.

23. (currently amended) An apparatus comprising:

a backplane communicatively connecting a cross-connect card to a device interface card;

means for receiving bits in multiple serial signals at a first bit rate from a—the backplane, the received bits representing data communicated between the cross-connect card and the device interface card;

means for converting the multiple serial signals to a parallel signal;

means for transmitting the parallel signal including the received bits at a second bit rate, wherein the second bit rate is greater than the first bit rate,

wherein stuffing data is removed from at least one of the multiple serial signals during conversion such that the number of the multiple serial signals multiplied by the second bit rate is equal to the first bit rate,

wherein the received bits are transmitted as SONET/SDH framed data in the parallel signal, and

wherein the receiving of bits in serial signals allows the backplane to be less complex.

Claims 24-25 (canceled)

26. (previously presented) The apparatus of claim 23 further comprising receiving the multiple serial signals at the first bit rate using both a first receiving circuit and a second receiving circuit.

27. (currently amended) The apparatus of claim ~~1~~ 37, wherein

the first bit rate corresponds to an STS-48 line rate,

the second bit rate corresponds to an STS-12 line rate, and

the number of transmitted serial signals is four.

28. (previously presented) The apparatus of claim 11, wherein

the first bit rate corresponds to an STS-48 line rate,

the second bit rate corresponds to an STS-12 line rate, and

the number of transmitted serial signals is four.

29. (previously presented) The apparatus of claim 15, wherein

the first bit rate corresponds to an STS-12 line rate,

the second bit rate corresponds to an STS-48 line rate, and

the number of received serial signals is four.

30. (previously presented) The apparatus of claim 19, wherein

the first bit rate corresponds to an STS-48 line rate,

the second bit rate corresponds to an STS-12 line rate, and

the number of transmitted serial signals is four.

31. (currently amended) The apparatus of claim ~~15~~ 23, wherein

the first bit rate corresponds to an STS-12 line rate,

the second bit rate corresponds to an STS-48 line rate, and

the number of received serial signals is four.

32. (currently amended) The apparatus of claim ~~1~~ 37, further comprising:

an interface to the backplane, wherein the backplane interface has a footprint whose size is configured for serial signals.

33. (previously presented) The method of claim 11, further comprising:

transmitting the multiple serials signals over the backplane via a footprint whose size is configured for serial signals.

34. (previously presented) The method of claim 15, further comprising:

receiving the multiple serial signals from the backplane via a footprint whose size is configured for serial signals.

35. (previously presented) The apparatus of claim 19, further comprising:

an interface to the backplane, wherein the backplane interface has a footprint whose size is configured for serial signals.

36. (previously presented) The apparatus of claim 23, further comprising:

an interface to the backplane, wherein the backplane interface has a footprint whose size is configured for serial signals.

37. (new) An apparatus comprising:

a backplane communicatively connecting a cross-connect card to a device interface card;

a parallel input/output line for sending and receiving bits;

a transmission circuit to transmit data over a backplane via one or more of a set of serial output lines, thereby communicating the data between the cross-connect card and the device interface card;

a receiving circuit to receive data over the backplane via one or more of a set of serial input lines; and

a parallel/serial conversion circuit operably coupled to the transmission circuit and to the receiving circuit, the parallel/serial conversion circuit being operable to:

convert SONET/SDH data, whose bits are received from the parallel input/output line at a first bit rate, from a parallel signal to multiple serial signals, thereby allowing the backplane to be less complex, and

send the converted multiple serial signals to the transmission circuit,

wherein:

the parallel/serial conversion circuit receives the SONET/SDH framed data at a first bit rate and converts the parallel signal to multiple serial signals at a second bit rate, the first bit rate being different than the second bit rate, and

the parallel/serial conversion circuit adds stuffing data to the received bits in the multiple serial signals, to allow the multiple serial signals to be transmitted at a second

bit rate, which is equal to the number of the multiple serial signals multiplied by the first bit rate, and

the transmission circuit transmits the multiple serial signals over the backplane at the second bit rate.

38. (new) The apparatus of claim 37, wherein the parallel/serial conversion circuit is further operable to receive one or more sets of serial signals from the receiving circuit, and convert the serial signals to a parallel signal.